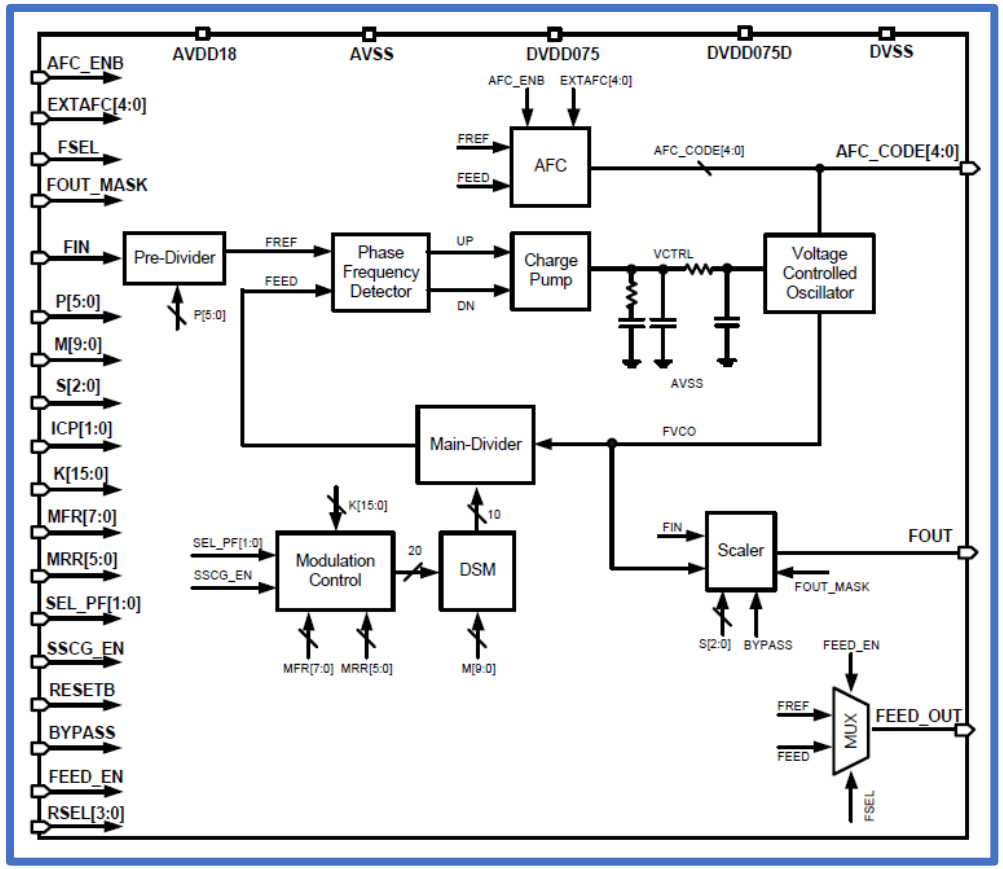
# PLL (sc_pllf0842x_ln08lpp)

## Block Diagram




## Features

- 8nm Low Power Plus (LN08LPP) CMOS device technology
- Dual power supply of 1.8V±10% and 0.85V+5% ~ 0.75V-10%
- Operating junction temperature(TJ): -40°C ~ 125°C
- Output frequency range: 35.2MHz ~ 4.5GHz
- Duty ratio: 48 ~ 52%
- Power down mode
- Area: 140µm x 181.608µm
- Bypass mode (FOUT = FIN)
- Programmable dividers
- Glitch-free scaler
- On-chip loop filter
  - Typical applications
  - Mobile/Consumer

## IP Status

- DK : Ready